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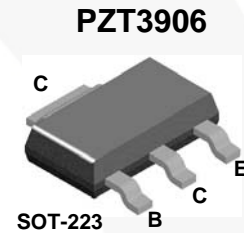
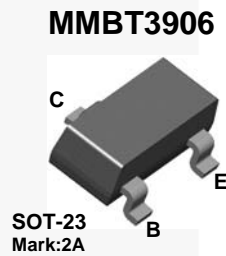
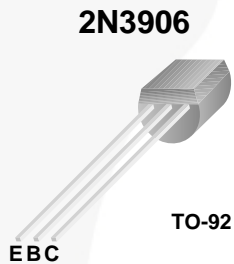


April 2014

## 2N3906 / MMBT3906 / PZT3906 PNP General-Purpose Amplifier

### Description

This device is designed for general-purpose amplifier and switching applications at collector currents of 10 mA to 100 mA.



### Ordering Information

Part Number	Marking	Package	Packing Method	Pack Quantity
2N3906BU	2N3906	TO-92 3L	Bulk	10000
2N3906TA	2N3906	TO-92 3L	Ammo	2000
2N3906TAR	2N3906	TO-92 3L	Ammo	2000
2N3906TF	2N3906	TO-92 3L	Tape and Reel	2000
2N3906TFR	2N3906	TO-92 3L	Tape and Reel	2000
MMBT3906	2A	SOT-23 3L	Tape and Reel	3000
PZT3906	3906	SOT-223 4L	Tape and Reel	2500

2N3906 / MMBT3906 / PZT3906 — PNP General-Purpose Amplifier

## Absolute Maximum Ratings<sup>(1)</sup>

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Value	Unit
$V_{CE0}$	Collector-Emitter Voltage	-40	V
$V_{CBO}$	Collector-Base Voltage	-40	V
$V_{EBO}$	Emitter-Base Voltage	-5.0	V
$I_C$	Collector Current - Continuous	-200	mA
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Note:

- These ratings are based on a maximum junction temperature of  $150^\circ\text{C}$ . These are steady-state limits. Fairchild Semiconductor should be consulted on applications involving pulsed or low-duty cycle operations.

## Thermal Characteristics

Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Maximum			Unit
		2N3906 <sup>(3)</sup>	MMBT3906 <sup>(2)</sup>	PZT3906 <sup>(3)</sup>	
$P_D$	Total Device Dissipation	625	350	1,000	mW
	Derate Above $25^\circ\text{C}$	5.0	2.8	8.0	$\text{mW}/^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	83.3			$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	200	357	125	$^\circ\text{C}/\text{W}$

### Notes:

- Device is mounted on FR-4 PCB 1.6 inch X 1.6 inch X 0.06 inch.
- PCB size: FR-4, 76 mm x 114 mm x 1.57 mm (3.0 inch x 4.5 inch x 0.062 inch) with minimum land pattern size.

## Electrical Characteristics

Values are at  $T_A = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Max.	Unit
<b>OFF CHARACTERISTICS</b>					
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage <sup>(4)</sup>	$I_C = -1.0\text{ mA}, I_B = 0$	-40		V
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	$I_C = -10\ \mu\text{A}, I_E = 0$	-40		V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	$I_E = -10\ \mu\text{A}, I_C = 0$	-5.0		V
$I_{BL}$	Base Cut-Off Current	$V_{CE} = -30\text{ V}, V_{BE} = 3.0\text{ V}$		-50	nA
$I_{CEX}$	Collector Cut-Off Current	$V_{CE} = -30\text{ V}, V_{BE} = 3.0\text{ V}$		-50	nA
<b>ON CHARACTERISTICS</b>					
$h_{FE}$	DC Current Gain <sup>(4)</sup>	$I_C = -0.1\text{ mA}, V_{CE} = -1.0\text{ V}$	60		
		$I_C = -1.0\text{ mA}, V_{CE} = -1.0\text{ V}$	80		
		$I_C = -10\text{ mA}, V_{CE} = -1.0\text{ V}$	100	300	
		$I_C = -50\text{ mA}, V_{CE} = -1.0\text{ V}$	60		
		$I_C = -100\text{ mA}, V_{CE} = -1.0\text{ V}$	30		
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_C = -10\text{ mA}, I_B = -1.0\text{ mA}$		-0.25	V
		$I_C = -50\text{ mA}, I_B = -5.0\text{ mA}$		-0.40	
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	$I_C = -10\text{ mA}, I_B = -1.0\text{ mA}$	-0.65	-0.85	V
		$I_C = -50\text{ mA}, I_B = -5.0\text{ mA}$		-0.95	
<b>SMALL SIGNAL CHARACTERISTICS</b>					
$f_T$	Current Gain - Bandwidth Product	$I_C = -10\text{ mA}, V_{CE} = -20\text{ V}, f = 100\text{ MHz}$	250		MHz
$C_{obo}$	Output Capacitance	$V_{CB} = -5.0\text{ V}, I_E = 0, f = 100\text{ kHz}$		4.5	pF
$C_{ibo}$	Input Capacitance	$V_{EB} = -0.5\text{ V}, I_C = 0, f = 100\text{ kHz}$		10.0	pF
NF	Noise Figure	$I_C = -100\ \mu\text{A}, V_{CE} = -5.0\text{ V}, R_S = 1.0\text{ k}\Omega, f = 10\text{ Hz to }15.7\text{ kHz}$		4.0	dB
<b>SWITCHING CHARACTERISTICS</b>					
$t_d$	Delay Time	$V_{CC} = -3.0\text{ V}, V_{BE} = -0.5\text{ V}$		35	ns
$t_r$	Rise Time	$I_C = -10\text{ mA}, I_{B1} = -1.0\text{ mA}$		35	ns
$t_s$	Storage Time	$V_{CC} = -3.0\text{ V}, I_C = -10\text{ mA}, I_{B1} = I_{B2} = -1.0\text{ mA}$		225	ns
$t_f$	Fall Time			75	ns

**Note:**

4. Pulse test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2.0\%$ .

## Typical Performance Characteristics

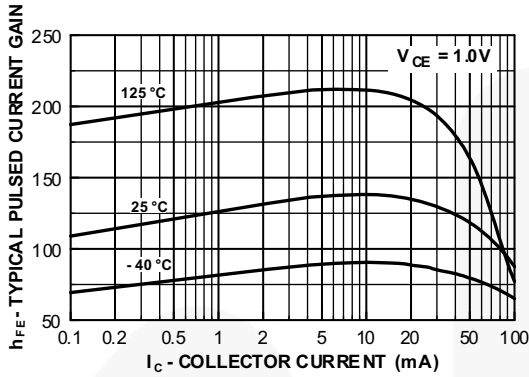


Figure 1. Typical Pulsed Current Gain vs. Collector Current

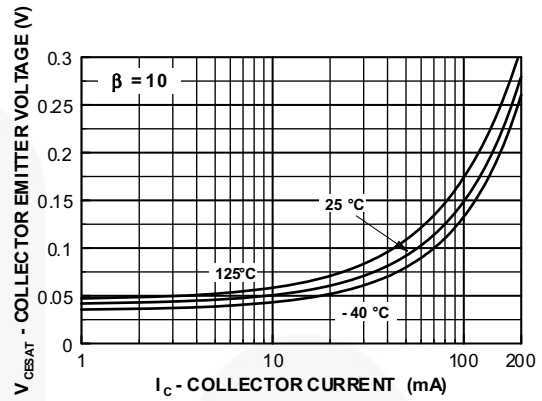


Figure 2. Collector-Emitter Saturation Voltage vs. Collector Current

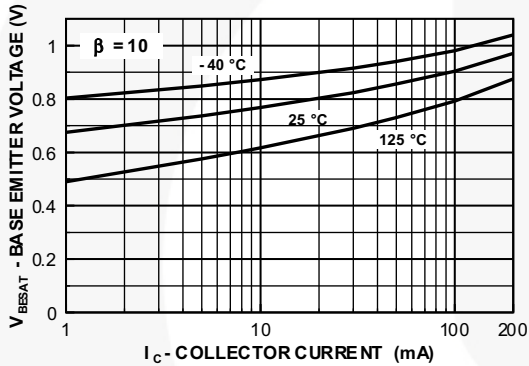


Figure 3. Base-Emitter Saturation Voltage vs. Collector Current

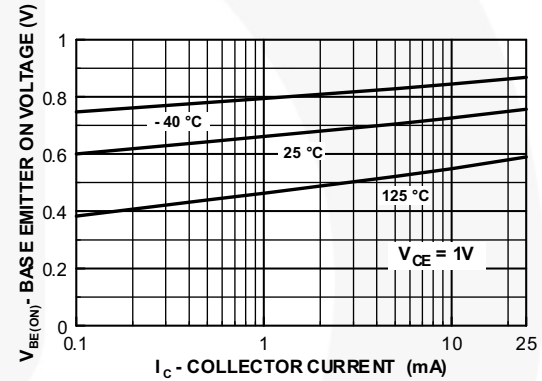


Figure 4. Base-Emitter On Voltage vs. Collector Current

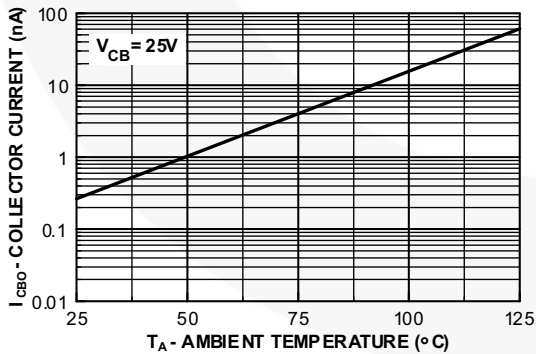


Figure 5. Collector Cut-Off Current vs. Ambient Temperature

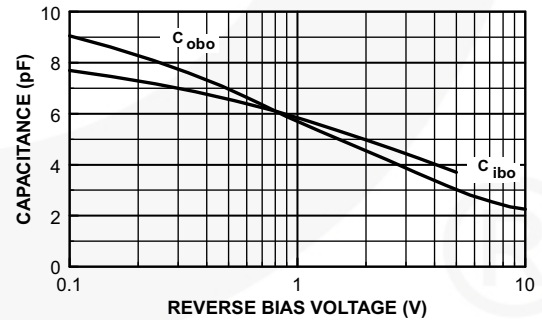


Figure 6. Common-Base Open Circuit Input and Output Capacitance vs. Reverse Bias Voltage

Typical Performance Characteristics (Continued)

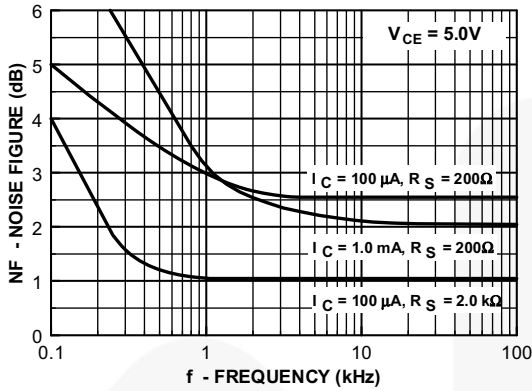


Figure 7. Noise Figure vs. Frequency

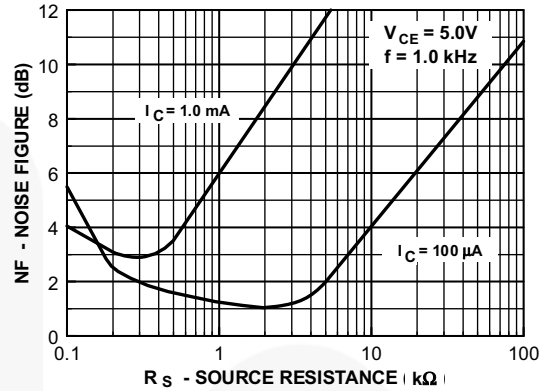


Figure 8. Noise Figure vs. Source Resistance

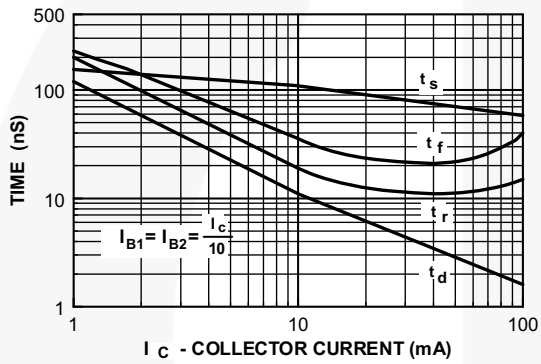


Figure 9. Switching Times vs. Collector Current

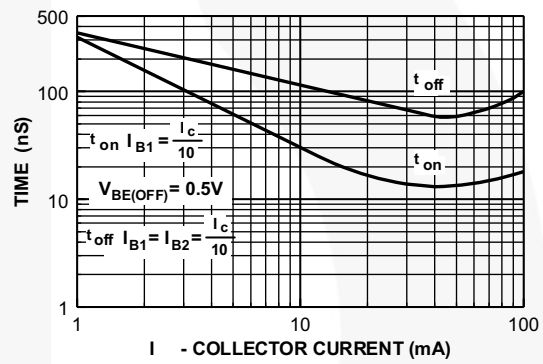


Figure 10. Turn-On and Turn-Off Times vs. Collector Current

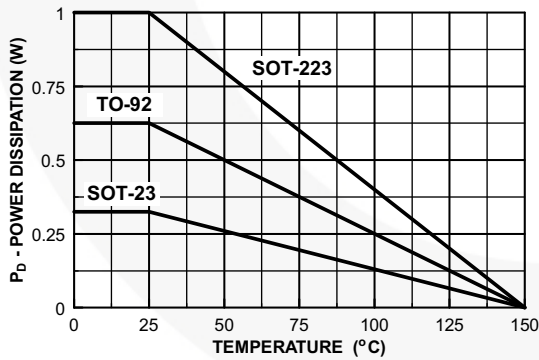


Figure 11. Power Dissipation vs. Ambient Temperature

Typical Performance Characteristics (Continued)

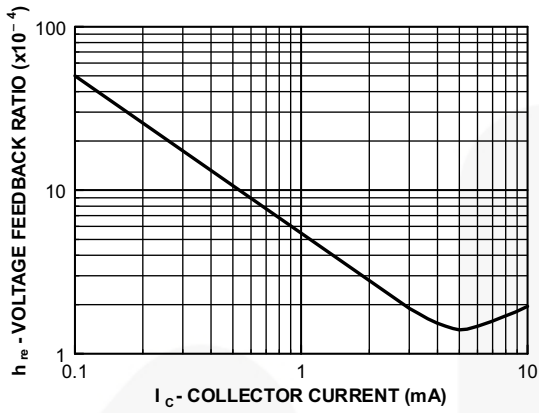


Figure 12. Voltage Feedback Ratio

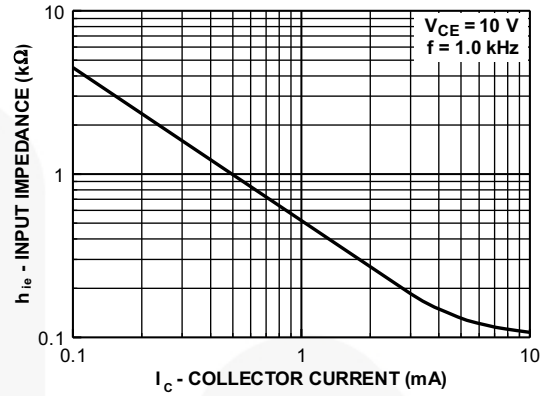


Figure 13. Input Impedance

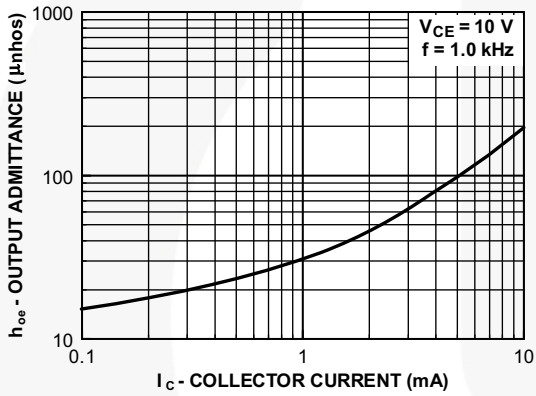


Figure 14. Output Admittance

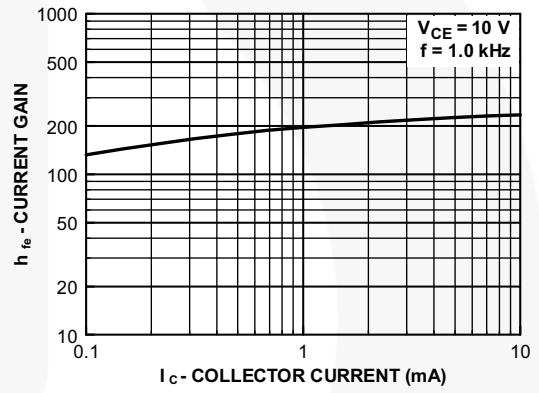
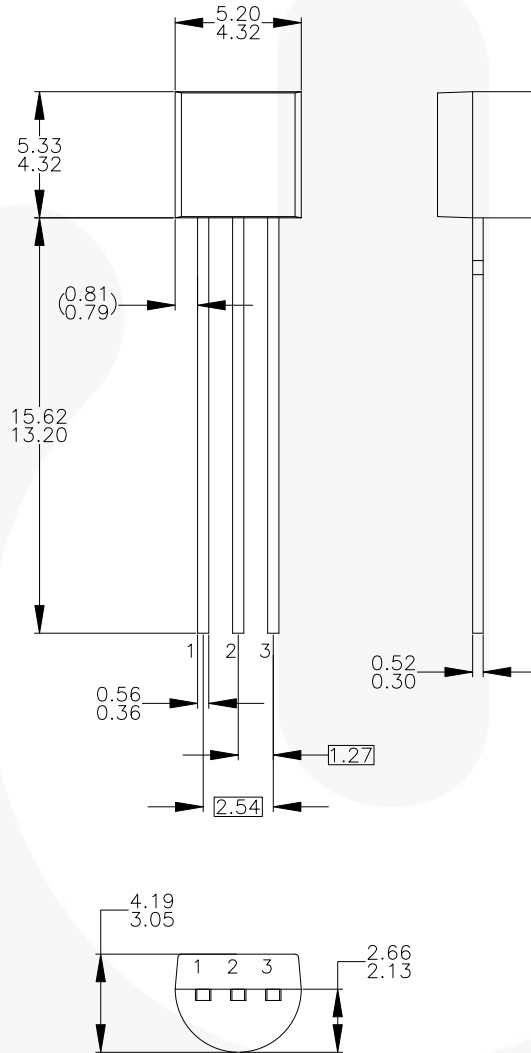


Figure 15. Current Gain

## Physical Dimensions

### TO-92 (Bulk)



NOTES: UNLESS OTHERWISE SPECIFIED

- A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DRAWING CONFORMS TO ASME Y14.5M-1994.
- D) TO-92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92			94			96			97			98		
	P	F	M	P	F	M	B	F	M	P	F	M	P	F	M
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

LEGEND:

P - BIPOLAR      E - EMITTER      D - DRAIN  
 F - JFET          B - BASE              S - SOURCE  
 M - DMOS        C - COLLECTOR      G - GATE

- E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEABLE AT JFET "F" OPTION.
- F) DRAWING FILENAME: MKT-ZA03DREV3.

**Figure 16. 3-LEAD, TO92, JEDEC TO-92 COMPLIANT STRAIGHT LEAD CONFIGURATION (OLD TO92AM3)**

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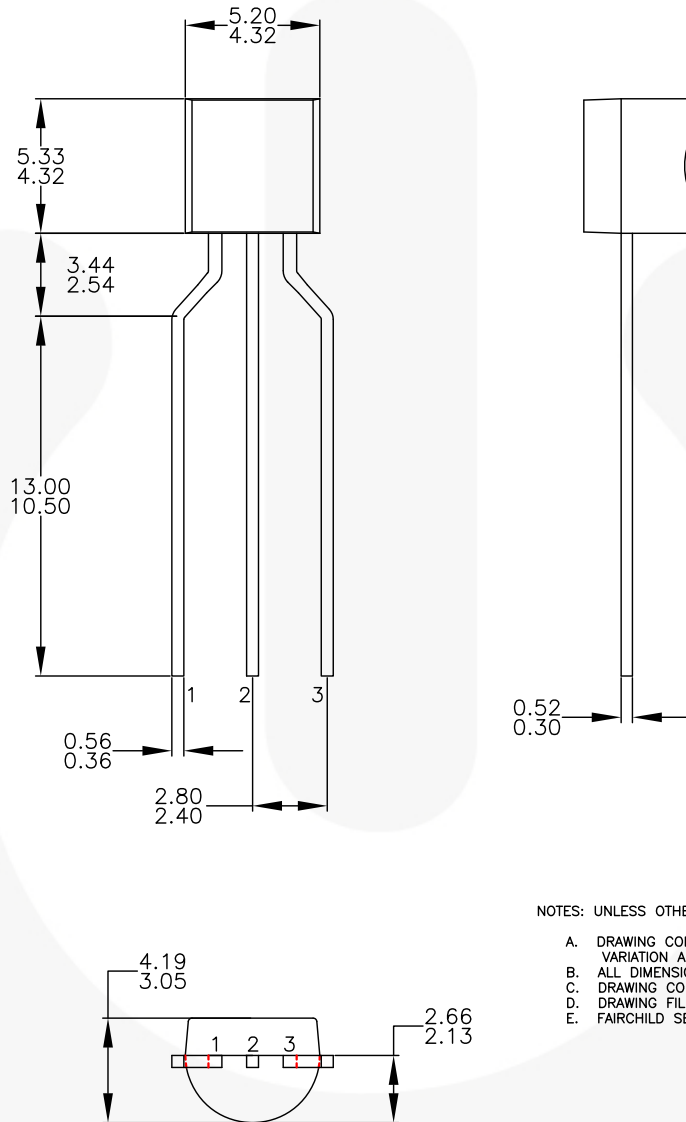
For current tape and reel specifications, visit Fairchild Semiconductor's online packaging area:

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Physical Dimensions (Continued)

TO-92 ( Ammo, Tape and Reel)



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- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DRAWING CONFORMS TO ASME Y14.5M-2009.
- D. DRAWING FILENAME: MKT-ZA03FREV3.
- E. FAIRCHILD SEMICONDUCTOR.

Figure 17. 3-LEAD, TO92, MOLDED 0.200 IN LINE SPACING LEAD FORM (J61Z OPTION)

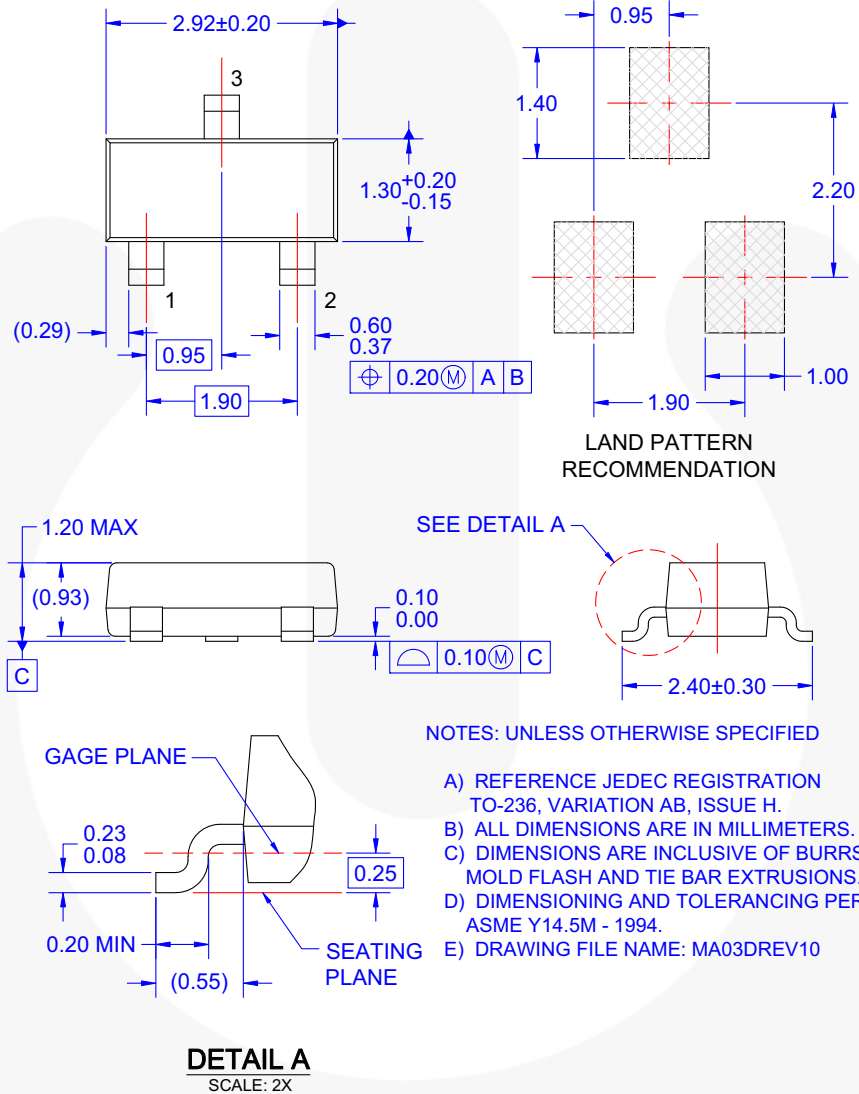
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[http://www.fairchildsemi.com/packing\\_dwg/PKG-ZA03F\\_BK.pdf](http://www.fairchildsemi.com/packing_dwg/PKG-ZA03F_BK.pdf)

**Physical Dimensions** (Continued)

**SOT-23**



**Figure 18. 3-LEAD, SOT23, JEDEC TO-236, LOW PROFILE**

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Physical Dimensions (Continued)

SOT-223 4L

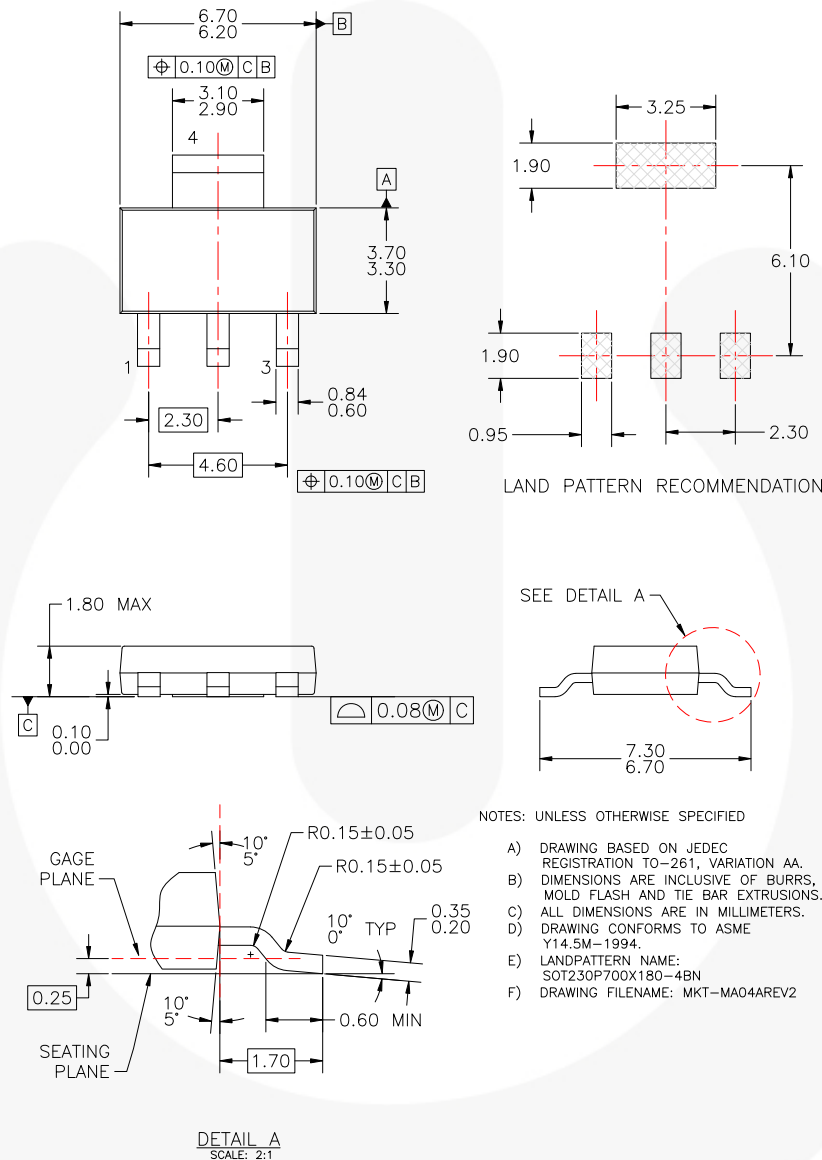


Figure 19. MOLDED PACKAGE, SOT-223, 4-LEAD

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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